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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/902,170	07/11/2001	Masahiko Ando	H6810.0011/P011	8805

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/902,170	ANDO ET AL.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-21,23-32,34,50-58,60-70,72-81 and 83* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-21,23-32,34,50-58,60-70,72-81 and 83* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 13, 2005 has been entered. A new rejection is made as set forth in this Office Action. Claims (1-9, 11-21, 23-32, 34, 50-58, 60-70, 72-81, and 83) are pending in the application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-8, 13-20, 24-31, 50-57, 62-69, and 74-80 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art of this application (AAPA) in view of Tsujimura et al. (U.S. Patent 6,391,691).

In re claims 1, 3, 5, 13, 24, and 50, **AAPA** discloses a method of fabricating a thin film transistor comprising the steps of (See Discussion of the Related Art on page 1-2 of this application and FIGS. 6(a)-(d)): providing a gate **62** over a substrate **61**; providing a gate insulating layer **63** over the gate and substrate; providing an amorphous silicon layer

64 having a first resistance over the gate insulating layer; providing an impurity on the surface of the amorphous silicon layer (FIGS. 6(a)-(b));

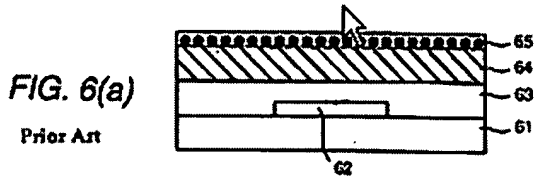


FIG. 6(a)
Prior Art

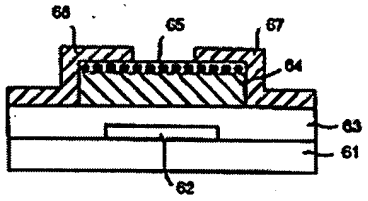


FIG. 6(b)
Prior Art

forming a drain electrode **66** and source electrode **67** separated by a channel region over a contact portion with the amorphous silicon layer; and subsequently, removing the impurity from the channel region (FIG. 6 (c)) to form a contact layer **65** within the amorphous silicon layer wherein the contact layer has a second resistance lower than the first resistance (page 2, lines 3-10); and

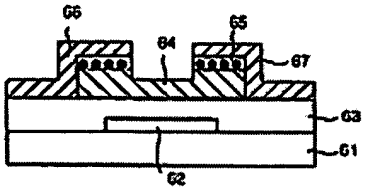


FIG. 6(c)
Prior Art

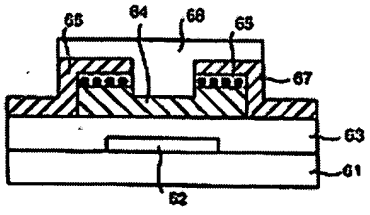


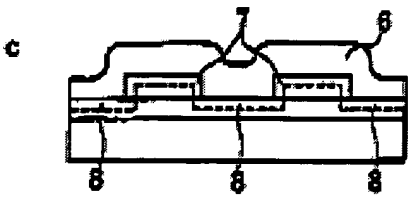
FIG. 6(d)
Prior Art

removing the impurity formed over the amorphous silicon **65** in the channel region between the drain **66** and source **67** electrodes while retaining the impurity over

the amorphous silicon film surface **64** contacted with drain **66** and source **67** region, so that the drain **66** and source **67** regions become a contact layer (Discussion of the Related Art, page 2, lines 6-18 and FIGS. 6(c)-(d)).

AAPA does not explicitly disclose diffusing the impurity into the contact portion to form the contact layer within the amorphous silicon layer.

Tsujimura, however, discloses a method of fabricating a thin film transistor comprising the steps (col. 3, line 46 to col. 4, line 19 and FIGS. 1-2): providing a gate **12** over a substrate **1**; providing a gate insulating layer **10** over the gate and substrate; providing an amorphous silicon layer **9** having a high resistance over the gate insulating layer; providing an impurity **7** and **8** on the surface of the amorphous silicon layer; forming a drain electrode **5** and source electrode **4** separated by a channel region over a contact portion with the amorphous silicon layer; and removing the impurity **8** from the channel region (col. 3, line 62 to col. 4, line 4 and FIG. 1(c)) and diffusing the impurity into the contact portion (col. 4, lines 6-19) to form a contact layer **11** within the amorphous silicon layer.



Therefore, It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of AAPA and Tsujimura to enable the process of diffusing the impurity into the contact portion to form a contact layer within the amorphous silicon layer of AAPA to be performed and furthermore to

achieve a good ohmic contact between source and drain electrodes and a semiconductor layer made of, for example, amorphous silicon in fabricating a thin film transistor (col. 1, lines 14-17, Tsujimura).

In re claims 2, 14, 25, 51, 63, and 74, **Tsujimura** discloses wherein the contact layer contains a concentration of the impurity of at least 0.1% (col.4, lines 6-19).

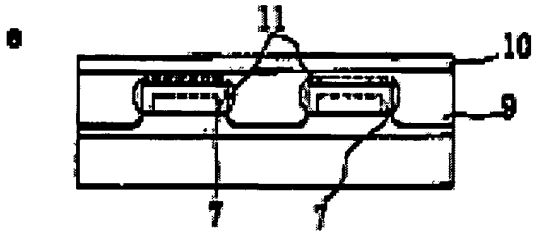
In re claims 3, 15, 26, 52, 64, and 75, **Tsujimura** discloses wherein removing of impurity from the channel region is performed by exposure to hydrogen plasma (col. 3, line 58 to col. 4, line 4).

In re claims 4, 6, 8, 16, 18, 20, 27, 29, 31, 53, 55, 57,65, 67, 69, 76, 78, and 80, **Tsujimura** discloses wherein the exposure is conducted for a time duration using a plasma chemical vapor deposition apparatus. There is no evidence indicating the hydrogen plasma exposure time duration, the heat annealing temperature and time duration, and the thickness of the amorphous silicon layer is critical and it has been held that it is not inventive to discover the optimum or workable temperature, time duration, and thickness of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

In re claims 5, 17, 28, 54, 66, and 77, **Tsujimura** discloses wherein the diffusion of the impurity into the contact portion is performing by heat annealing (col. 4, lines 4-19).

In re claims 7, 19, 30, 56, 68, and 79, **Tsujimura** discloses wherein the impurity is phosphorus (col. 3, line 58 to col. 4, line 4).

In re claim 13, **Tsujimura** discloses wherein the amorphous silicon layer **9** does not contain the impurity (col. 4, lines 6-19 and FIG. 1(e)).



In re claims 24, 62, and 73, **Tsujimura** discloses wherein essentially none of the impurity is diffused into the contact portion prior to removing step (col. 3, line 46 to col. 4, line 19).

In re claims 50, 62, and 73, **Tsujimura** discloses a method of fabricating a liquid crystal display (LCD) comprising the steps of providing a plurality of thin film transistors arranged on a LCD substrate in a matrix form (col. 4, lines 6-57).

2. Claims 9, 11-13, 21, 23, 24, 32, 34, 58, 60-62, 70, 72, 73, 81, and 83 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art of this application (AAPA) in view of Tsujimura et al. (U.S. Patent 6,391,691) as applied to claims 1-8, 13-20, 24-31, 50-57, 62-69, and 74-80 above, and further in view of Washizuka et al. (IDW 1997 pp. 207-210).

In re claims 9, 11, 21, 32, 58, 62, 70, 73, and 81, **Washizuka** discloses wherein the diffusing step is performed simultaneously with an annealing step for a capping layer provided over the electrode and the channel region and wherein etching the amorphous silicon layer utilizing a common photoresist to form the electrodes (page 208 and FIGS. 2-3).

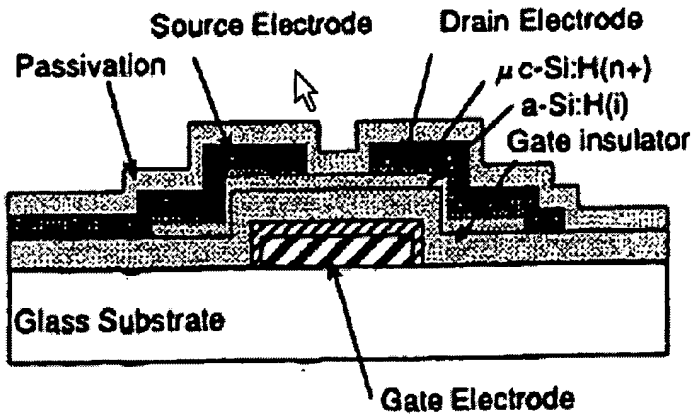


Figure 2 Cross sectional view of the inverted staggered a-Si TFT of back channel etching type used in this study

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of AAPA, Tsujimura, and Washizuka to achieve high image quality of TFT-LCDs (page 207, Washizuka).

In re claims 12, 23, 34, 61, 72, and 83, **Washizuka** discloses wherein the steps are entirely conducted by using an etching apparatus and a protection film forming apparatus while connected in a vacuum state (page 208 and FIGS. 2-3).

In re claims 13, 24, and 60, **Washizuka** discloses wherein etching the silicon layer utilizing a common photoresist to form a drain electrode and a source electrode

separated by a channel region over a contact portion with amorphous silicon layer (page 208 and FIGS. 2-3).

Response to Applicants' Arguments and Amendment

Applicants contend that neither AAPA (the applicants' admitted prior art) nor Tsujimura (U.S. Patent 6,391,691) herein known as AAPA and Tsujimura, either alone or in combination, disclose or suggest the step of "removing the impurity formed over the amorphous silicon in the channel region between the drain and source electrodes while retaining the impurity over the amorphous silicon film surface contacted with drain and source region."

In response to Applicants' contention that neither AAPA nor Tsujimura, either alone or in combination, disclose or suggest the step of "removing the impurity formed over the amorphous silicon in the channel region between the drain and source electrodes while retaining the impurity over the amorphous silicon film surface contacted with drain and source region.", Examiner respectfully disagrees. Applicants are directed to the Specification under (Discussion of the Related Art, page 2, lines 6-18 and FIGS. 6(c)-(d)) where AAPA discloses removing the impurity formed over the amorphous silicon **65** in the channel region between the drain **66** and source **67** electrodes while retaining the impurity over the amorphous silicon film surface **64** contacted with drain **66** and source **67** region, so that the drain **66** and source **67** regions become a contact layer (Discussion of the Related Art, page 2, lines 6-18 and FIGS. 6(c)-(d)).

For this reason, Examiner holds the rejection proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
November 9, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER